**DESIGN OF EFFICIENT 64 BIT MAC UNIT USING VEDIC MULTIPLIER FOR DSP APPLICATION – A REVIEW**

**Abstract:**

Multiplier Accumulator Unit (MAC) is a part of Digital Signal Processors. The speed of MAC depends on the speed of multiplier. The proposed MAC unit reduces the area by reducing the number of multiplication and addition in the multiplier unit. Increase in the speed of operation is achieved by the hierarchical nature of the Vedic multiplier unit. So by using an efficient Vedic multiplier which excels in terms of speed, power and area, the performance of MAC can be increased. For this fast method of multiplication based on ancient Indian Vedic mathematics is used. Among various method of multiplication in Vedic mathematics, Urdhva Tiryagbhyam is used and the multiplication is for 64 X 64 bits. Urdhva Tiryagbhyam is a general multiplication formula applicable to all cases of multiplication. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros.

**Keywords**— MAC, Vedic Multiplier, VHDL, Ripple Carry (RC) Adder

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**