**SCAN TEST BANDWIDTH MANAGEMENT FOR ULTRA LARGE SCALE SYSTEM-ON-CHIP ARCHITECTURES**

**Abstract:**

This paper presents several techniques employed to resolve problems surfacing when applying scan bandwidth management to large industrial multicore system-on-chip (SoC) designs with embedded test data compression. These designspose significant challenges to the channel management scheme, flow, and tools. This paper introduces several test logic architectures that facilitate preemptive test scheduling for SoC circuits with embedded deterministic test-based test data compression. The same solutions allow efficient handling of physical constraints in realistic applications. Finally, stateof-the-art SoC test scheduling algorithms are rearchitected accordingly by making provisions for: 1) setting up timeeffective test configurations; 2) optimization of SoC pin partitions; 3) allocation of core-level channels based on scan data volume; and 4) more flexible core-wise usage of automatic test equipment channel resources. A detailed case study is illustrated herein with a variety of experiments allowing one to learn how to tradeoff different architectures and test-related factors.

**Keywords:** SoC, Data Compression, Design-For-Test (DFT).

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**