**LOW-POWER AND AREA-EFFICIENT SHIFT REGISTER USING PULSED LATCHES**

**Abstract:**

This paper proposes a low-power and area-efficient shift register using digital pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using a 0.18µm CMOS process with VDD = 1.8V. The core area is 6600µm2. The power consumption is 1.2mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops. In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the ―data‖ input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the ―bit array‖ stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. More generally, a shift register may be multidimensional, such that it‘s ―data in‖ and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

**Keywords**: Area-Efficient, Flip-Flop, Pulsed Clock, Pulsed Latch, Shift Register.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**