**DELAY EFFICIENT ERROR DETECTION AND CORRECTION OF PARALLEL IIR FILTERS USING VLSI ALGORITHMS**

**Abstract:**

Almost all electronic systems suffer from errors caused by various internal and external factors. In many designs automatic detection and correction of errors is of prime importance. In the meantime the techniques that add to detect and correct errors will make the system more sluggish. This paper proposes a method for error detection and correction in parallel IIR filters based on error correction codes. Even though a lot of studies have been done with FIR filters, the area of IIR filters have received very less attention. The reason for this is design of an IIR filter is much complicated than an FIR filter due to its recursive nature. Scaling and roundoff error plays a major role and special care must be taken to overcome this. To improve the speed of the system, the conventional adders and multipliers are replaced with carry select adder and Booth multiplier. The effectiveness of the scheme is shown in terms of error protection, hardware utilization and delay. A remarkable reduction in delay is obtained through the application of these algorithms.

**Keywords** - Error correction codes (ECCs), Parallel filters, Carry Select Adder, Booth Algorithm, Delay efficiency.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**