**DESIGN AND IMPLEMENTATION OF 64 BIT VEDIC MULTIPLIER USING ADDERS (VERILOG HDL)**

**Abstract:**

This Paper describes the design of high speed Vedic multiplier that uses the techniques of Vedic mathematics based on 16 sutras (algorithms) to improve the performance. In this work the efficiency of Urdhva-Tiryagbhyam (vertical and crosswise) Vedic method for multiplication which is different from the process of normal multiplication is presented. Urdhva-Tiryagbhyam is the most efficient algorithm that gives minimum delay for multiplication for all types of numbers irrespective of their size. Vedic multiplier is coded in Verilog HDL and stimulated and synthesized by using XILINX software 14.7v ISE on Spartan 3E kit. Further the design of Vedic multiplier is design with Hybrid adder and compared with the proposed multiplier in terms of delay, power and device utilization.

**Keywords -** Vedic mathematics, Vedic multiplier, Urdhva-Tiryagbhyam, Ripple Carry Adder (RCA), Binary to Excess Code Converter (BEC), Half Adder (HA), Full Adder(FA), Carry Select Adder (CSLA), parallel Prefix adders, Brent Kung adder.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**