**A NEW VLSI ALGORITHM FOR A HIGH-THROUGHPUT IMPLEMENTATION OF TYPE IV DCT**

**Abstract:**

A new design approach based on a new VLSI algorithm for high speed applications of a prime length type IV discrete cosine transform that uses short length cycle convolution structures is presented. It uses a new parallel decomposition method of type IV discrete cosine transform (DCT) that leads to a high throughput VLSI implementation with a low hardware cost. The proposed algorithm is efficiently mapped onto two linear systolic arrays. A VLSI implementation with good performances can be obtained that has a modular and regular structure with a a low I/O cost and local and regular interconnections.

**Keywords—**VLSI algorithms, discrete transforms, DCT-IV, systolic arrays.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**