**DESIGN OF DELAY EFFICIENT MODIFIED 16 BIT WALLACE MULTIPLIER**

**Abstract:**

The structure of modified tree multipliers with different adders is presented. Multiplication is an important fundamental arithmetic operation in all microprocessor circuits and algorithms. Currently the speed of multipliers is limited by the speed of adders used for partial products addition. In this paper Conventional Array Multiplier and Dadda Multiplier are compared with the Wallace multiplier in terms of delay. Further a proposed sixteen bit Wallace multiplier is implemented by using Carry Select Adder (CSLA) and Binary to Excess -1 Converter (BEC) adder. The delay for Wallace multiplier using CSLA is less when compared to Wallace multiplier with BEC. These multipliers are coded in Verilog HDL, simulated and synthesized by using XILINX software 12.2 on Spartan 3E FPGA device xc3s500-5fg320.

**Keywords**— Array Multiplier, Wallace Multiplier, Dadda Multiplier, Proposed Multiplier, Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Binary to Excess Code Converter-1 (BEC-1),Half Adder (HA),Full Adder(FA).

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**