**AN EFFICIENT VLSI ARCHITECTURE FOR DATA ENCRYPTION USING AES ALGORITHM AND ITS FPGA IMPLEMENTATION**

**Abstract:**

To accomplish the objective of secure correspondence, cryptography is one of the best fundamental activity. The more well known and broadly received symmetric encryption calculation prone to be experienced now a days is AES (Advanced Encryption Standard) calculation .It is found no less than 6 times quicker than old AES calculation. AES is an iterative as opposed to Feistel Cipher. It depends on substitution stage organize. Parallelization idea utilizes different assets to take care of substantial and complex issue. Throughput is increased by sub-pipelining and by number of different pipelining stages.

**KEYWORDS**: Cryptography, pipelining, AES-algorithm, Fiestel cipher, FPGA

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**