**ANALYSIS AND DESIGN OF LOW-POWER REVERSIBLE CARRY SELECT ADDER USING D-LATCH**

**Abstract:**

Most important design parameter in integrated circuit is Power dissipation after speed. Adders are one of the basic fundamental component in such circuit, designing much efficient Adder results in optimizing whole circuit. Due to rapid growth in technology there is a need of fast processing arithmetic unit, so Carry Select Adder (CSLA) is one of the fast processing adder. By observing the CSLA circuitry it is noticed that, further optimization can be achieved in various criteria. Power dissipation results only when bits are lost while processing, as per Launder’s principle, KTln2 heat is dissipated if there is any loss in bit. Since conventional CSLA is designed using irreversible logic gates which it results much more power dissipation but it can be overcome by employing reversible logic to reduce power dissipation till some extent. By using this idea, following paper proposes a efficient technique to design 8-bit CSLA using reversible logic, for this purpose this paper undertakes 8-bit CSLA with D Latch.. This paper evaluates the proposed design in-terms of power, delay, garbage output, quantum cost and number of gates using 90nm CMOS process technology for nbits. All the works related to proposed design carried in cadence virtuoso tool and by comparing the simulation results and analysis this paper observed that, proposed reversible CSLA using D-latch attains low power dissipation which is equal to 94.68uW,which shows decrease in 59.175%than irreversible

CSLA using D-latch.

**Keywords**:Carry Select Adder (CSLA),Quantum Cost (QC), Garbage Outputs (GO), Fredkin gate (F), Peres Gate (PG), Feynman gate(FG), Reversible D Flip Flop(RDF), Reversible MUX(RMUX), Reversible Ripple carry adder (RRCA),Ripple carry adder (RCA), Reversible full adder (RFA) .

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**