**ADDITION OF MILLER AND INVERTED MANCHESTER ENCODING TECHNIQUE TO DEDICATED SHORT RANGE COMMUNICATION WITH FULL HARDWARE UTILIZATION**

**Abstract:**

The dedicated short-range communication (DSRC) plays important role in modern intelligent transportation system. The DSRC standards generally adopt FM0 and Manchester encoding technique to reach dc balance and enhance the signal reliability. Same properties are possessed by Miller and inverted Manchester encoding. Therefore, this two techniques can be added in existing FM0/Manchester encoding module. By using conventional technique of modelling results in huge coding diversity with hardware utilization rate of 57.14%. Similarity oriented logic simplification (SOLS) technique is used to overcome this limitation and achieve 100% hardware utilization rate. Hardware utilization and optimization capability of this paper is evaluated on Xilinx ISE Design Suit 13.1 simulation software and design implemented on Xilinx sparten-3E FPGA kit. The encoder architecture in this paper is based on DSRC standards of America, Europe and Japan. This paper develops fully utilized VLSI architecture with two additional and compatible encoding techniques. It also provides efficient performance compared with the existing work.

**Keywords—** Dedicated Short Range Communication (DSRC), FM0, Manchester, Miller, Similarity Orientation Logic Simplification (SOLS

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**