**MULTIPLIERS-DRIVEN PERTURBATION OF COEFﬁCIENTS FOR LOW-POWER OPERATION IN RECONﬁGURABLE FIR FILTERS**

**Abstract:**

 Reconﬁgurable ﬁnite-impulse response (FIR) ﬁlters are one of the most widely implemented components in Internet of Things systems that require ﬂexibility to support several target applications while consuming the minimum amount of power to comply with the strict design requirements of portable devices. Due to the signiﬁcant power consumption in the multiplier components of the FIR ﬁlter, various techniques aimed at reducing the switching activity of these multipliers have been proposed in the literature. However, these techniques rarely exploit the ﬂexibility on the algorithmic level, which can lead to additional beneﬁts. In this paper, FIR ﬁlter multipliers are extensively characterized with power simulations, providing a methodology for the perturbation of the coefﬁcients of baseline ﬁlters at the algorithm level to trade-off reduced power consumption for ﬁlter quality. The proposed optimization technique does not require any hardware overhead and it enables the possibility of scaling the power consumption of the ﬁlter at runtime, while ensuring the full baseline performance of any programmed ﬁlter whenever it is required. The analyzed FIR ﬁlters were fabricated in a 28nm FD-SOI test chip and measured at a near-threshold, 600mV supply voltage. For example, by carefully choosing slightly perturbed coefﬁcients in a low-pass conﬁguration, power savings of up to 33% are achieved when accepting a 3dB degradation on the stopband, as compared with the baseline implementation of the ﬁlter.

**Index Terms**—VLSI signal processing, FIR ﬁlters, digital multipliers, low-power design, approximate computing

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**