VLSI MAJOR PROJECT LIST

1. An Efficient Implementation of Floating Point Multiplier.
2. Design and Simulation of UART Serial Communication Module Based on VHDL.
3. Design of FPGA-Based Traffic Light Controller System.
4. 32 Bit×32 Bit Multiprecision Razor-Based Dynamic Voltage Scaling Multiplier With Operands Scheduler.
5. A Parallel-Serial Decimal Multiplier Architecture.
6. Design and Implementation of Automated Wave-Pipelined Circuit using ASIC.
7. Design of Low Power TPG Using LP-LFSR.
8. Low-Power and Area-Efficient Carry Select Adder.
9. A High Speed Binary Floating Point Multiplier Using Dadda Algorithm.
10. Design a DSP Operations using Vedic Mathematics.
11. Design High Speed Low Power Multiplier using Reversible logic.
12. Design High Speed Low Power Multiplier using Reversible logic a Vedic Mathematical Approach.
13. Design of High Performance 64 bit MAC Unit.
14. High Performance Hardware Implementation of AES Using Minimal Resources.
15. Implementation and Comparison of Effective Area Efficient Architectures for CSLA.
16. Implementation of I2C Master Bus Controller on FPGA.
17. Low-Power, High-Throughput, and Low-Area Adaptive FIR Filter Based on Distributed Arithmetic.
18. Novel High Speed Vedic Mathematics Multiplier using Compressors.
19. Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic.
20. An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator.
21. Area-Delay Efficient Binary Adders in QCA.

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22. Bit-Level Optimization of Adder-Trees for Multiple Constant Multiplications for Efficient FIR Filter Implementation.
23. Design and Development of FPGA Based Low Power Pipelined 64-Bit RISE Processor with Double Precision Floating Point Unit.
24. Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata.
25. High Speed Convolution and Deconvolution Algorithm.
26. High-Throughput Multistandard Transform Core Supporting MPEGH.264VC-1 Using Common Sharing Distributed Arithmetic.
27. Implementation Of Floating Point Mac Using Residue Number System.
28. Verification of Four Port Router for NOC.
29. A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications.
30. Design and Development of FPGA Based Low Power.
31. A Novel Area-Efficient VLSI Architecture for Recursion Computation in LTE Turbo Decoders.
32. Efficient Coding Schemes for Fault-Tolerant.
33. High Speed Fir Filter Designs Based On Booth Multipler.
34. Low-Power and Area-Efficient Shift Register Using Recursive Approach to the Design of a Parallel Self-Timed Adder.
35. An Area- and Energy-Efficient FIFO Design Using Error-Reduced Data Compression and Near-Threshold Operation for Image/Video Applications.
36. An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis.
37. Area-Delay-Power Efficient Fixed-Point LMS Adaptive Filter With Low Adaptation-Delay.
38. Design of Improved Performance Voltage Controlled Ring Oscillator.

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39. Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm.
40. Data Encoding Techniques for Reducing Energy.
41. Consumption in Network-on-Chip.
42. Efficient FPGA Implementation of Address Generator for WiMAX Deinterleaver.
43. Efficient Parallel Architecture for Linear Feedback Shift Registers.
44. Efficient VLSI Architecture for Decimation-in-Time Fast Fourier Transform of Real-Valued Data.
45. Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells.
46. Low-cost and high-speed hardware implementation of contrast-preserving image dynamic range compression for full-HD video enhancement.
47. Low-Power and Area-Efficient Shift Register Using Pulsed Latches.
48. Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations.
49. RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing.

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