VLSI MAJOR PROJECT LIST

1. A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits.
2. Memory-Reduced Turbo Decoding Architecture Using NII Metric Compression.
3. Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication.
4. A Novel Structure for Rayleigh Channel Generation With Consideration of the Implementation in FPGA.
5. Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units.
6. LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter
7. RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing
8. Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation
9. A Configurable Parallel Hardware Architecture for Efficient Integral Histogram Image Computing
10. A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications.
11. A Cellular Network Architecture With Polynomial Weight Functions
12. A Binaural Neuromorphic Auditory Sensor for FPGA: A Spike Signal Processing Approach
13. A Low-Power Broad-Bandwidth Noise Cancellation VLSI Circuit Design for In-Ear Headphones
14. In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers.
15. Concept, Design, and Implementation of Reconfigurable CORDIC.
16. A Novel Coding Scheme for Secure Communications in Distributed RFID Systems.

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17. An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis.

18. Low-cost and high-speed hardware implementation of contrast-preserving image dynamic range compression for full-HD video enhancement.

19. Low-Power and Area-Efficient Shift Register Using Pulsed Latches.

20. Reconfigurable Filter Bank With Complete Control Over Sub band Bandwidths for Multistandard Wireless Communication Receivers.

21. High-Throughput Digit-Level Systolic Multiplier Over GF (2*m*) Based on Irreducible Trinomials.

22. Aggressive Voltage Scaling Through Fast Correction of Multiple Errors with Seamless Pipeline Operation.

23. A Low-Power Architecture for the Design of a One- Dimensional Median Filter.

24. Aging-aware Reliable multiplier design with adaptive hold logic.

25. An Area- and Energy-Efficient FIFO Design Using Error- Reduced Data Compression and Near-Threshold Operation for Image/Video Applications.

26. Efficient Parallel Architecture for Linear Feedback Shift Registers.

27. Result-Biased Distributed-Arithmetic-Based Filter Architectures for Approximately Computing the DWT.

28. Reconfigurable Filter Bank With Complete Control Over Sub-band Bandwidths for Multi standard Wireless Communication Receivers.

29. Vectored Implementation of Hierarchical 22*n* QAM.

30. Normalized Sub-band Adaptive Filtering Algorithm with Reduced Computational Complexity.

31. A PFD and Charge Pump Switching Circuit to Optimize the Output Phase Noise of the PLL in 90 nm CMOS **(Backend)**

32. Design and Analysis of an Adaptively Biased Low Dropout Regulator Using Enhanced Current Mirror Buffer **(Backend)**

33. Design of Improved Performance Voltage Controlled Ring Oscillator **(Backend)**

34. Analysis and Design of Dual-Mode CMOS LC-VCOs**(Backend)**

35. Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power Supply Rejection**(Backend)**
36. Area Delay Efficient Binary Adders in QCA.
37. Input vector monitoring concurrent BIST Architecture using SRAM cells.
38. Area-delay-power efficient fixed point LMS Adaptive filter with low adaptation delay.
39. Efficient FPGA Implementation of Addresses generator for WiMAX Deinterleaver.
40. .Low complexity Low Latency Architecture for matching of data encoded with hard systematic error correcting codes.
41. Reverse converter design via parallel prefix adders: Novel components, methodology and implementations.
42. Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip.
43. Critical path analysis & low complexity implementation of the LMS adaptive algorithm.
44. An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator.